

FIG. 1

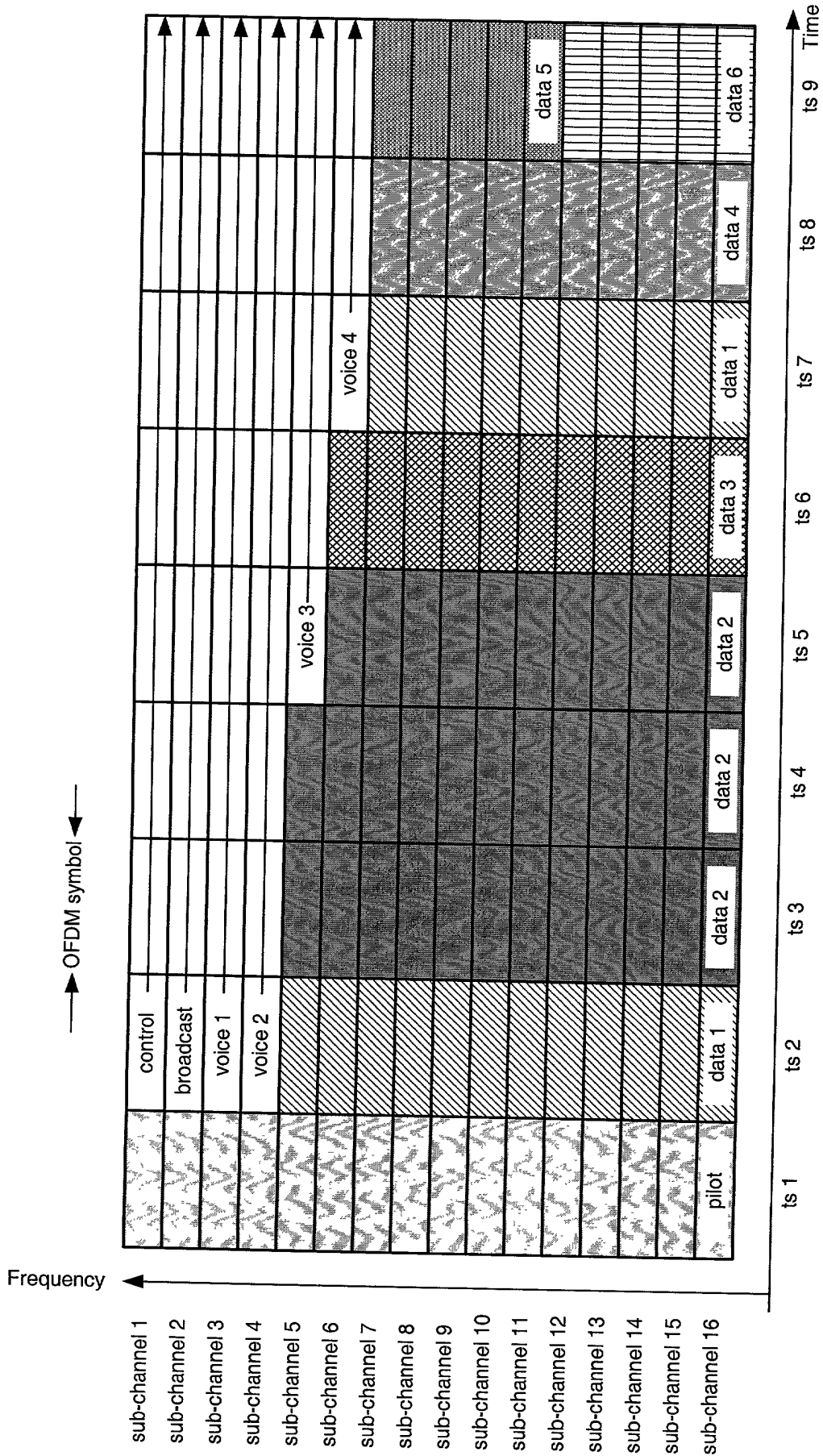


FIG. 2

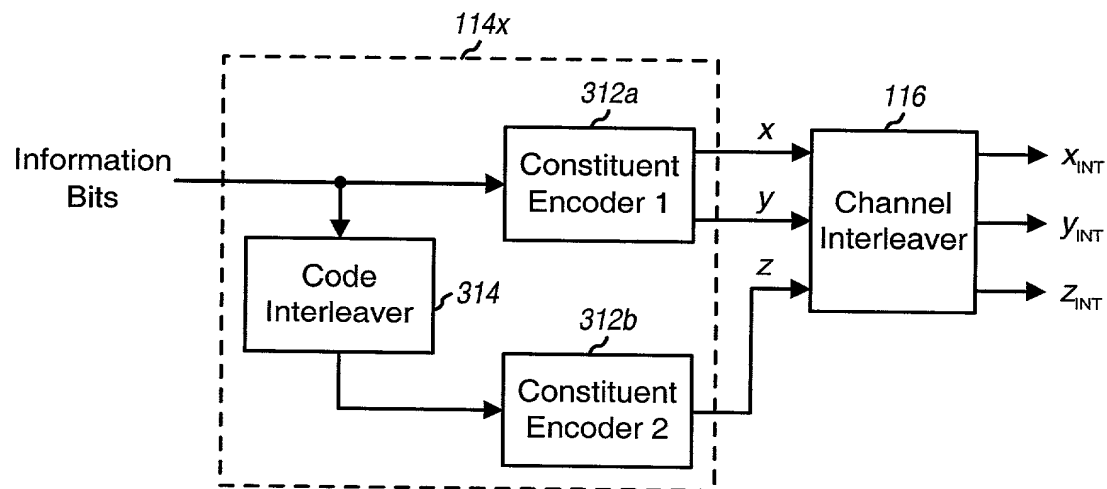


FIG. 3A

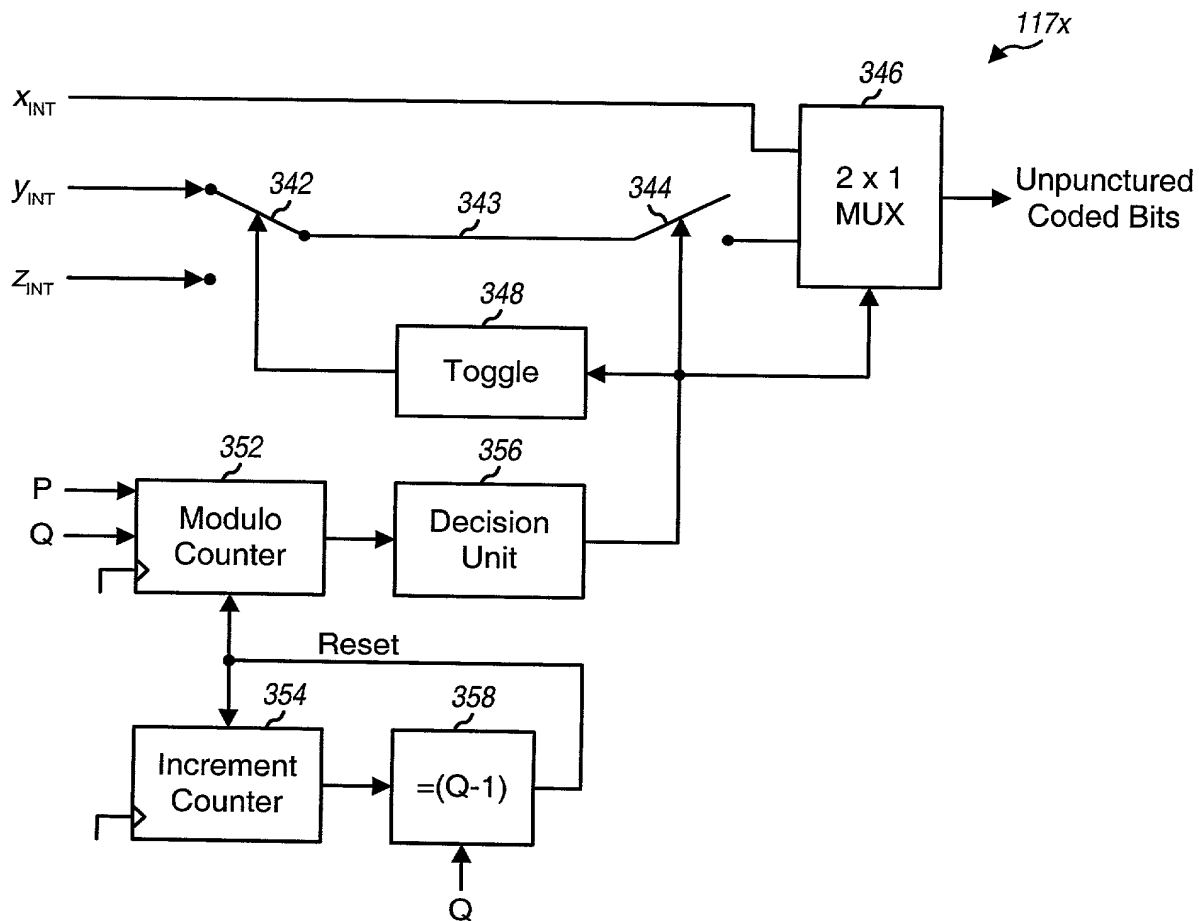


FIG. 3C

FIG. 3B is a block diagram of a system 114y for processing information bits. The system 114y includes a Code Interleaver 314 and a Channel Interleaver 116. The system 114y also includes a feedback loop 322a and a feedback loop 322b. The system 114y is configured to process information bits and generate intermediate signals x_{INT}, y_{INT}, and z_{INT}.

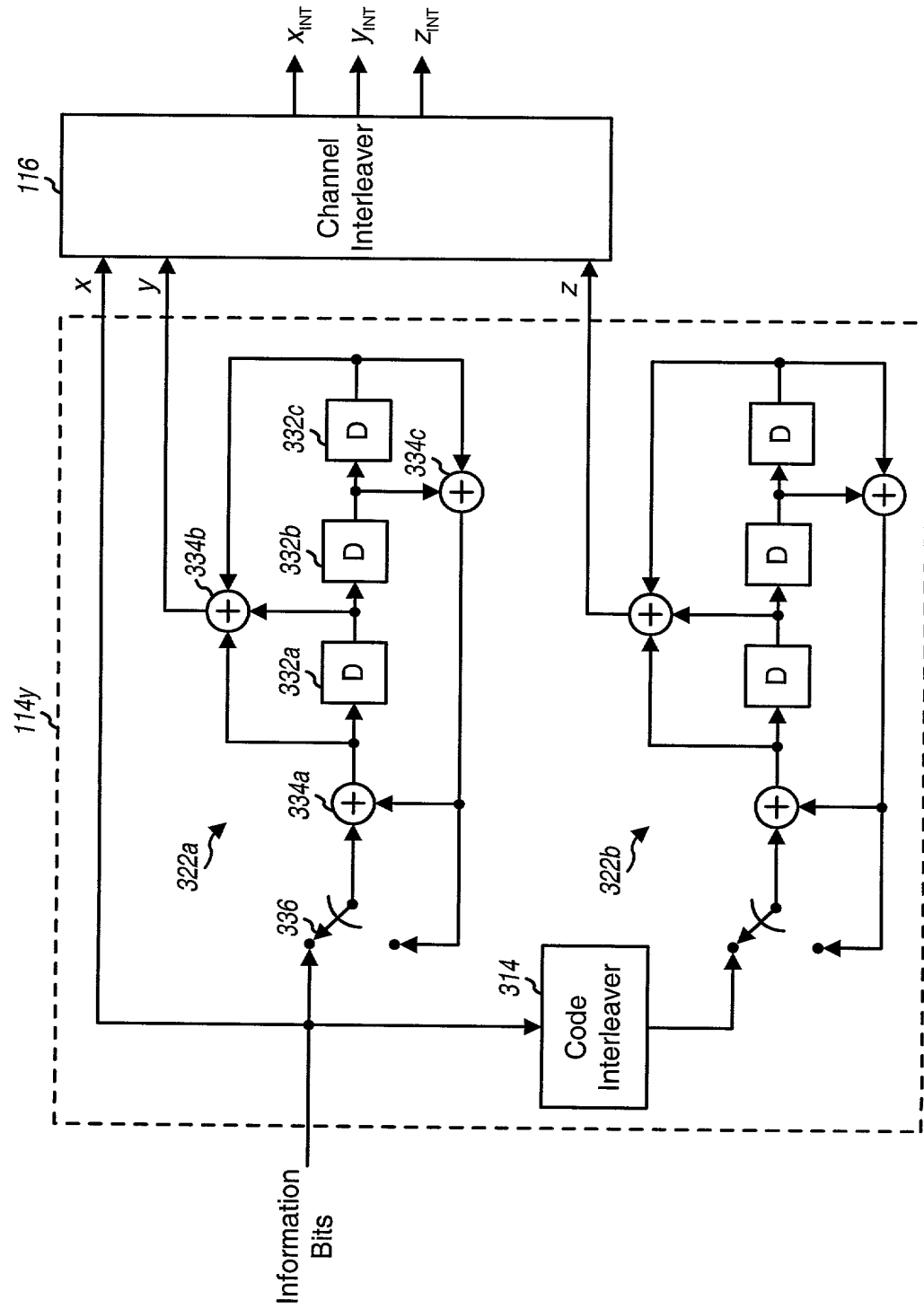


FIG. 3B

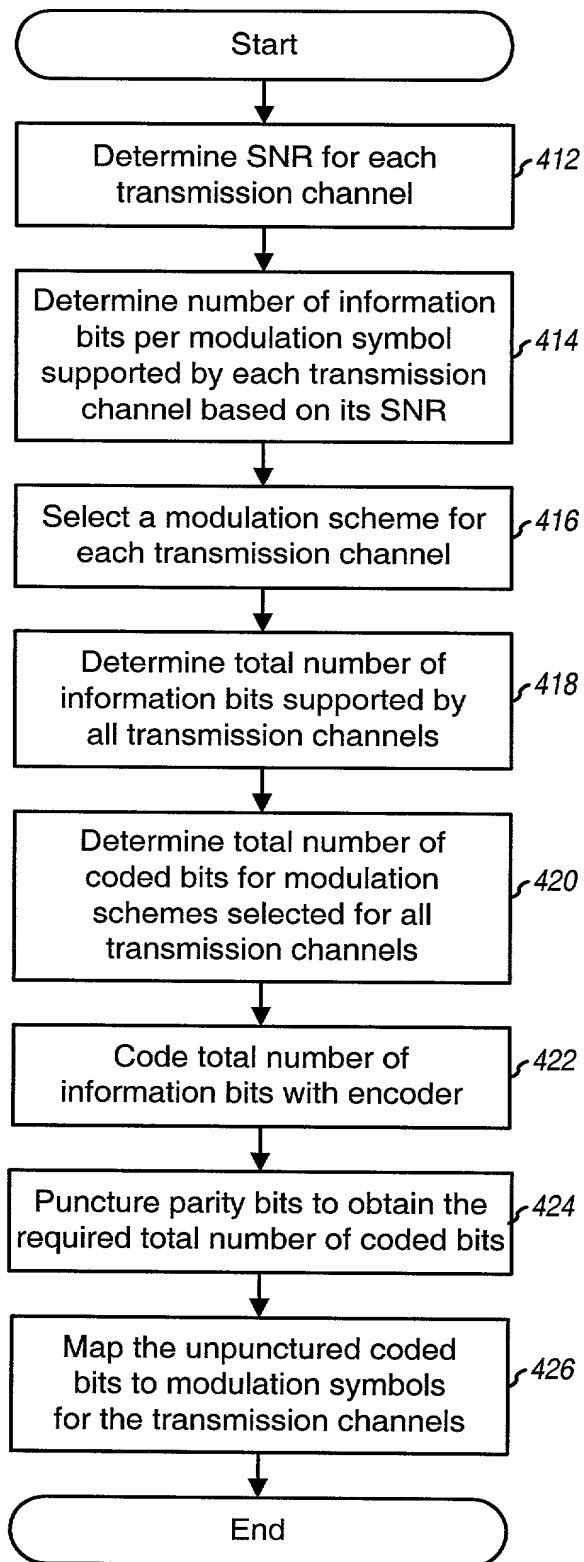


FIG. 4A

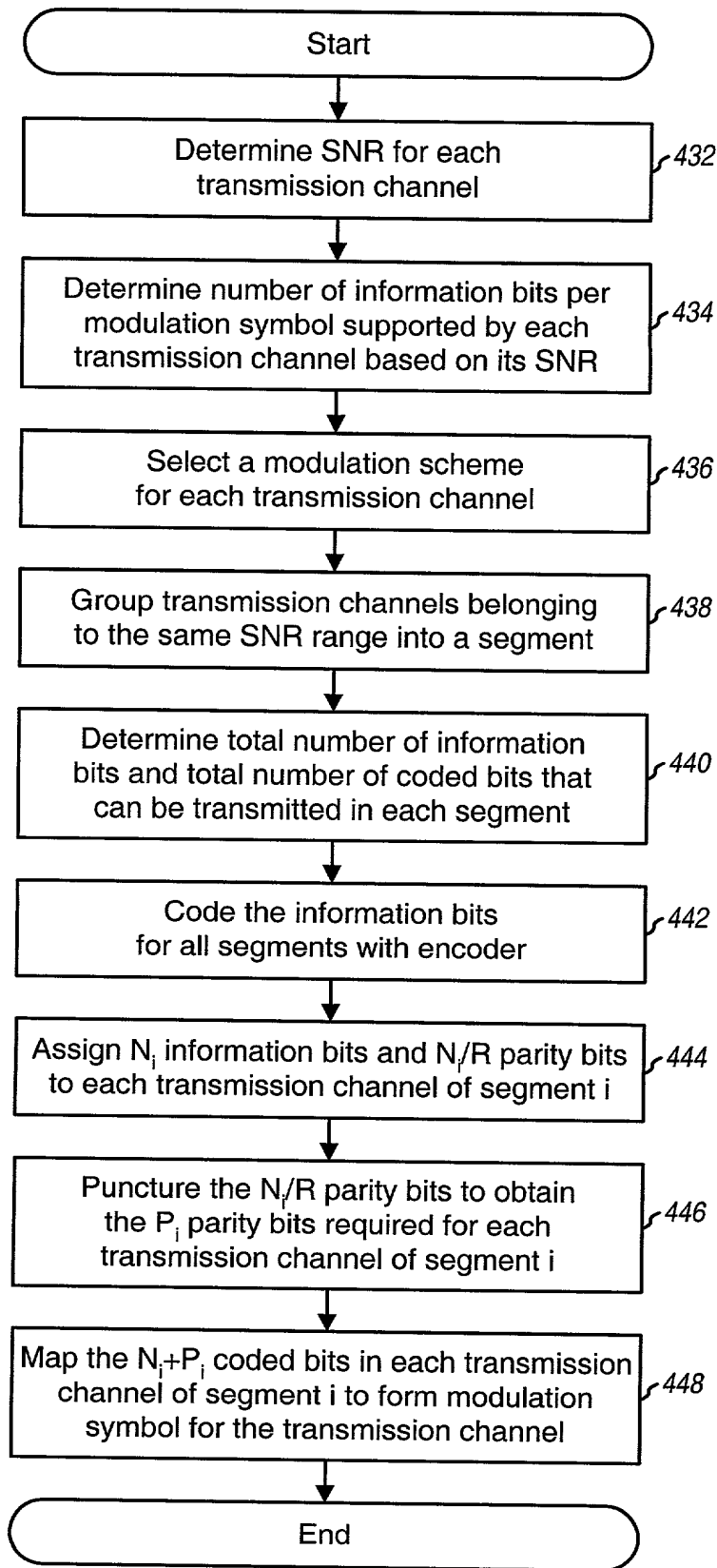


FIG. 4B

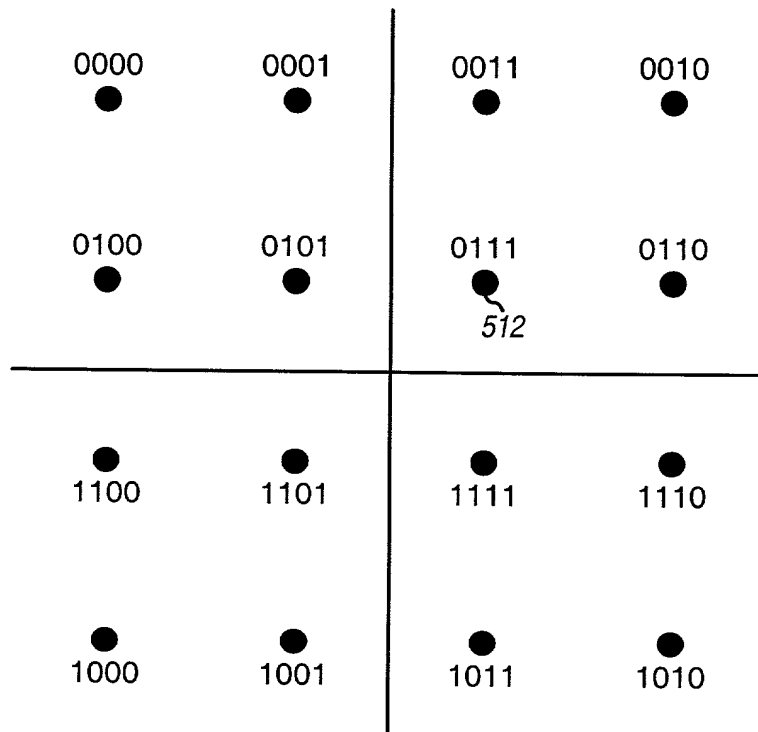
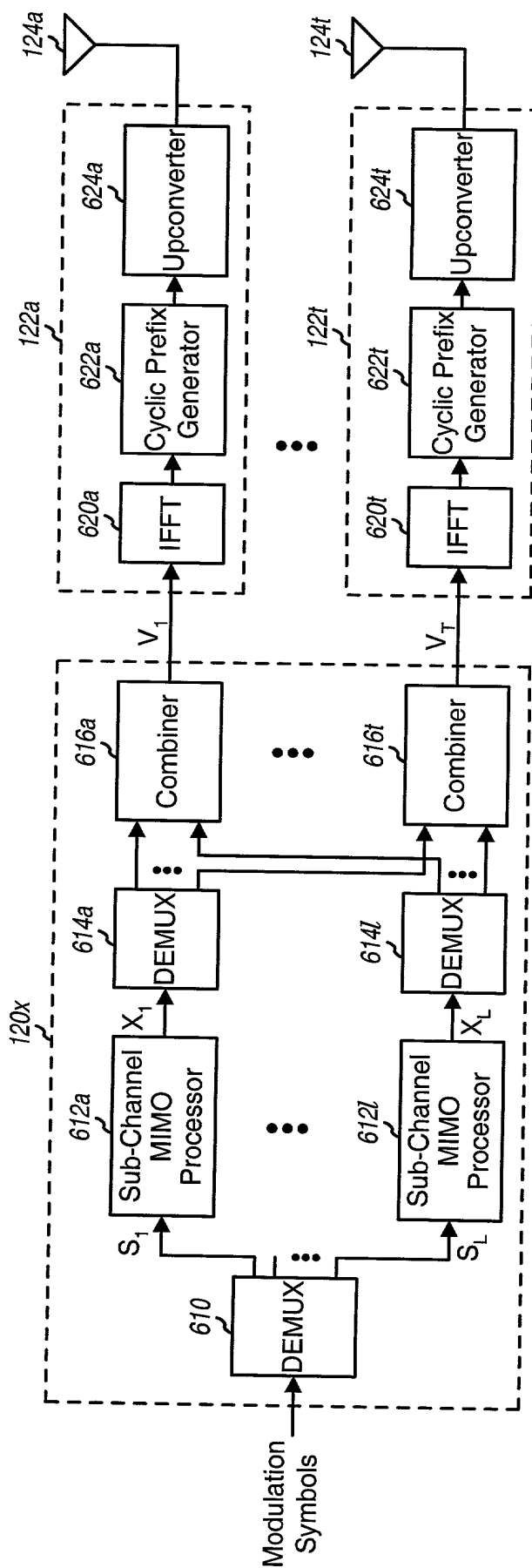


FIG. 5



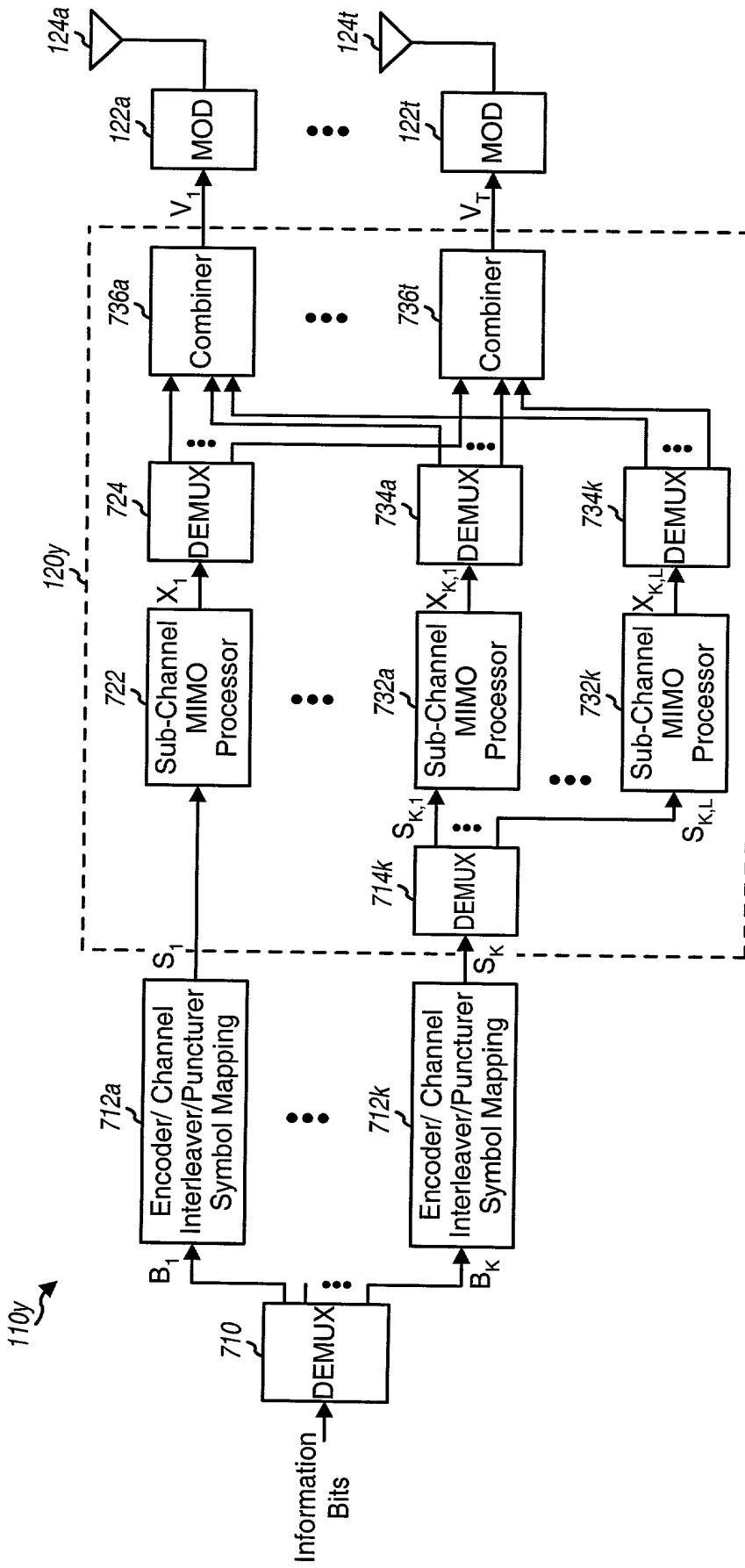


FIG. 7

FIG. 8 is a block diagram of a receiver system 162x. The system includes a Bit LLR Calculation block 158x, a De-Puncturer block 159, and a Channel Deinterleaver block 160. The system also includes a Detector block 818, a Code Interleaver block 814, a Decoder block 812b, a Code Deinterleaver block 816, and two Decoder blocks 812a and 810b. The system is configured to process Received Modulation Symbols and output Decoded Bits.

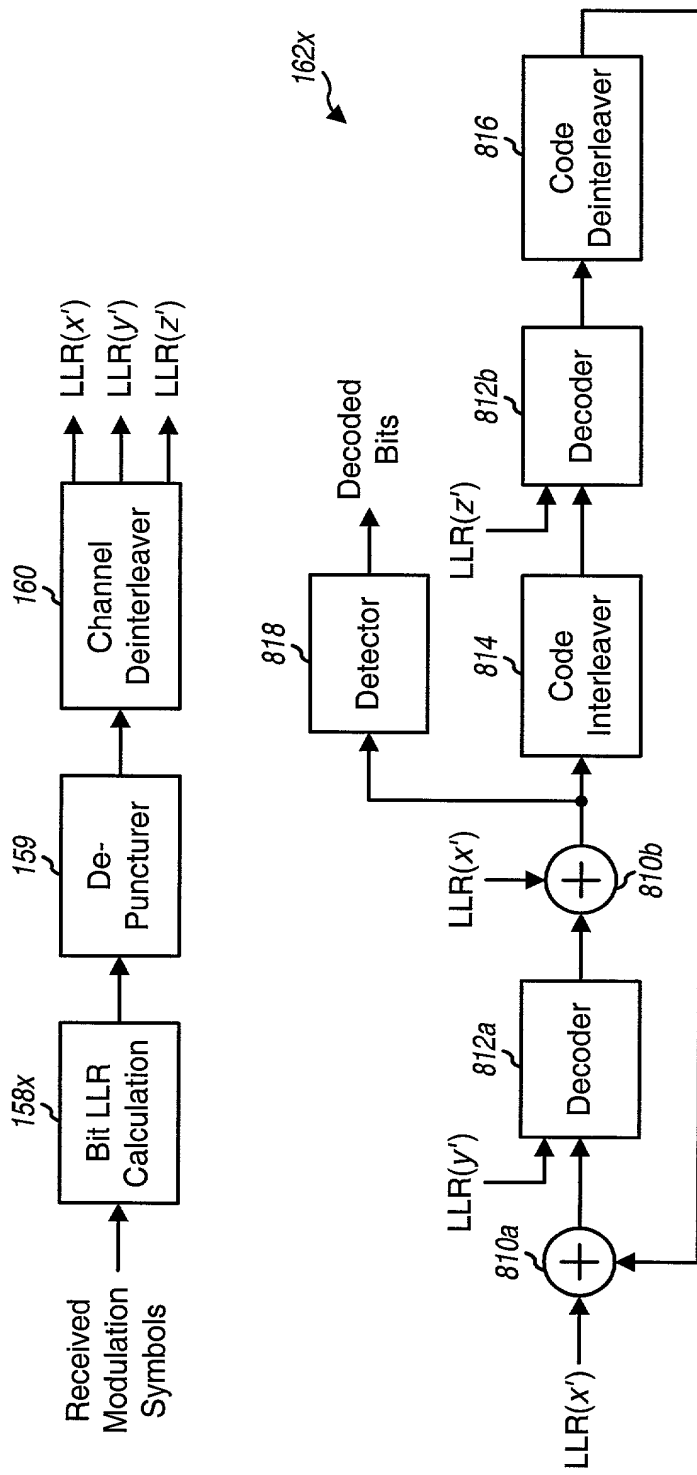


FIG. 8